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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/576,708	04/21/2006	Mamoru Tsuruya	289328US2PCT	2093
22850	7590	03/18/2008	EXAMINER	
OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, P.C.			HANSEN, STUART ALAN	
1940 DUKE STREET			ART UNIT	PAPER NUMBER
ALEXANDRIA, VA 22314			2838	
			NOTIFICATION DATE	DELIVERY MODE
			03/18/2008	ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/576,708	TSURUYA, MAMORU	
	<b>Examiner</b>	<b>Art Unit</b>	
	STUART HANSEN	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 17 January 2008.  
 2a) This action is **FINAL**.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-19 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-19 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 21 April 2006 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) Notice of References Cited (PTO-892)  
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  
 3) Information Disclosure Statement(s) (PTO/SB/08)  
 Paper No(s)/Mail Date 1/17/2008.

4) Interview Summary (PTO-413)  
 Paper No(s)/Mail Date. \_\_\_\_\_.  
 5) Notice of Informal Patent Application  
 6) Other: \_\_\_\_\_.

## DETAILED ACTION

1. This Office Action is in response to the Amendments/Arguments filed January 17<sup>th</sup>, 2008.

### ***Claim Rejections - 35 USC § 103***

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1, 3, 10 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshikawa (JP 08-205539) in view of Umminger et al. (US 2002/0180413). Yoshikawa teaches: A boost reactor (Fig 1 [L1]) which receives power from a rectified AC input voltage (10, 11) for correcting power factor (Paragraph 20); a main switch which is turned on and off (Q1; Paragraph 11); a converting section which turns the input voltage into smooth output DC voltage (D5, C1); and a control section (3) which controls the main switch to output a specific voltage according to a switch current (R1, G; Paragraphs 16 – 19), wherein the control section comprises: an error amplifier (30, 31) which amplifies an error between the output voltage (A from 2) and a first reference voltage (B) to generate an error voltage signal (C'; Paragraph 12); a current detection amplifying section (R1, G, 4 and CP1) which amplifies an error between a voltage which is proportional to the current detected by the current detection section, and a second reference voltage (F) to output a voltage amplifying signal (H); a frequency control section (34, 35, and CP1); a voltage varying section (33) which outputs a voltage signal (F) obtained by varying the voltage amplifying signal of the

current detection amplifying section (output of CP1 affects F as it affects the feedback signal A) according to a value of the error voltage signal from the error voltage generating section as the second reference voltage (F) to the current detection amplifying section (CP1) and a pulse width control section (36) which controls based on the error voltage and the frequency control section and applies the pulse to the main switch. Yoshikawa however fails to teach: the control section controls both a switching frequency and a switching duty cycle of the main switch. Umminger et al. however does teach a DC-DC converting circuit (Fig 3A) with a controller (10, 34) which controls a switching frequency and duty cycle of a main switch (13, 15; Paragraphs 4, 10 and 13). Umminger et al. and Yoshikawa both teach voltage conversion devices therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a combination of both frequency and duty cycle modulation as is taught in Umminger et al. in the power factor correcting DC-DC converter of Yoshikawa.

4. Claims 4 – 6, 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshikawa in view of Umminger et al. as applied to claim 1 above, and further in view of Hwang (US 2003/0222627). Yoshikawa in view of Umminger et al. teaches: the control section reduces the switching frequency of the main switch when the current in the main switch decreases. Yoshikawa in view of Umminger et al. however fails to teach: the control section sets the switching frequency to a lower limit minimum frequency when the average main switch current is at or below a lower limit current setting or to an upper limit maximum frequency when the main switch current is at or above an upper limit current setting, and the control section stops switching operation of

the main switch when the current is below a lower limit or an average value of the main switch current is less than or equal to a limit value, and that switching starts again when the output voltage falls to a limit voltage. Hwang though teaches: the control section sets the switching frequency to a lower limit frequency when the average current flowing from the rectifier is at or below a lower limit current setting or to an upper limit when the average current flowing from the rectifier is at or above an upper limit; the frequency control section also having an upper limit if the current approaches an upper limit setting; and the control section stops switching operation of the main switch when the average current is below a lower limit, and that switching starts again when the output voltage falls to a limit voltage (Paragraphs 12, 19, 38, 61, 81; input current can fall to zero indicating, at low load levels, the switching frequency is 0Hz, or very nearly that, and that the switching is stopped). Hwang teaches pulse frequency and width modulation and also that the supply circuit, which is very similar to that of Yoshikawa in view of Umminger et al., has certain limits as to the current of the main switch, the energy stored in the reactor and the frequency at which the switch is operated and how they relate to one another, therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the frequency modulation techniques, and system current, voltage and frequency limits of Hwang with the system of Yoshikawa in view of Umminger et al. for the purpose of better system control and increased system security by protecting system devices with said operating limitations.

5. Claims 2, 11 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshikawa in view of Umminger et al. and Peron (US 2004/0113596). Yoshikawa

in view of Umminger et al. teaches all claimed subject matter previously addressed in claims 1, 3 and 10. Yoshikawa in view of Umminger et al. fails to teach, however: a boost reactor with primary and coupled feedback winding and includes a leakage inductance more than a predetermined inductance value (all windings exhibit a leakage inductance more than some value); a first series circuit from the one rectifier output to the other, and includes the primary winding a first diode and a smoothing capacitor; a second series circuit from the one rectifier output to the other which includes the primary winding, the feedback winding and a main switch; and a second diode connected between a junction of the main switch and the feedback winding and the smoothing capacitor. Peron, though, does teach: a boost reactor with primary (Fig 5 [L0]) and loosely coupled feedback winding (L); a first series circuit from one output (2) to the other (5), and includes the primary winding (L0) a first diode (DL) and a smoothing capacitor (C0); a second series circuit from one output to the other which includes the primary winding (L0), the feedback winding (L) and a main switch (K); and a second diode (D1) connected between a junction of the main switch (K) and the feedback winding (L) and the smoothing capacitor (C0). Peron and Yoshikawa in view of Umminger et al. both teach voltage conversion devices therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the boost reactor with the primary and loosely coupled feedback windings with the feedback diode of Peron in place of the boost reactor of Yoshikawa for the purpose of increasing the overall maximum amount of energy capable of being stored in the system reactance, allowing for higher efficiency and more effective power transfer. Another

obvious means would be to have the feedback winding fully coupled to the primary winding, increasing the magnetic coupling ratio and further increasing energy transfer.

6. Claims 12 – 14, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshikawa in view of Umminger et al. and Peron as applied to claim 2 above, and further in view of Hwang. Claims 12 – 14, 16 and 17 are identical to claims 4 – 6, 8 and 9 and are therefore rejected as previously stated regarding the claimed subject matter also in claims 4 – 6, 8 and 9.

7. Claims 7 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshikawa in view of Umminger et al. as applied to claim 1, or alternatively Yoshikawa in view of Umminger et al. and Peron as applied to claim 2 above, and further in view of Chinomi et al. (JP 10-174428). Yoshikawa in view of Umminger et al. and Yoshikawa in view of Umminger et al. and Peron both fail to teach: that the boost reactor inductance value reduces when the value of the current flowing into the boost reactor is increased. Chinomi et al. however, teaches: the boost reactor (Fig 1 [2]) inductance value is adjustable according to the load current (Paragraph 33). Chinomi et al. teaches a conversion circuit similar to that of Yoshikawa in view of Umminger et al. and Peron, also with adjustable switching frequency, therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made that the inductance value of the boost reactor of Yoshikawa in view of Umminger et al. and Peron be adjustable according to the load current such as that of Chinomi et al. for the purpose of increasing power transfer efficiency.

***Response to Arguments***

8. Applicant's arguments and amendments, filed January 17<sup>th</sup>, 2008, with respect to the rejections of claims 1 – 18 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection has been made in view of Umminger et al. Applicant was correct that Yoshikawa did not teach simultaneous pulse frequency and pulse width variability. Umminger et al. however corrects this deficiency. Applicants arguments regarding the voltage varying section Yoshikawa not getting feedback from the current detection amplifier is incorrect because the current detection amplifier has a direct correlation to the output voltage and therefore affects the feedback signal to the voltage varying section.

***Conclusion***

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Karlsson (US 5,654,626), Jovanovic (US 5,736,842), Hussein et al. (US 2004/0263134), Chiu (US 2006/0012359), Ye (US 7,012,413), Sankman et al. (US 7,046,528) and Kawashima (JP 08019259) all teach voltage regulation systems similar to the present application.

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stuart Hansen whose telephone number is (571) 270-1611. The examiner can normally be reached on 8-5:30 Mon - Thurs, every 2nd Fri 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Akm Ullah can be reached on (571) 272-2361. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Stuart Hansen  
March 19, 2008 /S. H./  
Examiner, Art Unit 2838

/Jeffrey L. Sterrett/  
Primary Examiner, Art Unit 2838